

Technical Note

WDGA SSI Basics

Stand: 20.03.2017

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1. General information

This technical note is to assist all those who deal with the products stated above.

This technical note serves as an example of a functioning application. A liability is excluded for material and legal errors in this documentation, especially for their accuracy, correctness, freedom from intellectual property and rights of third parties, completeness and/or usability in cases of intent or malice.

To ensure a safe operation, the device may be operated only according to the instructions of the operating manual. When used, the legal and security provisions are also to be observed for each specific application. This also applies when using accessories.

2. SSI Basic

The position value is transmitted MSB first. The length of the SSI process data value has the length of the position value (Ordered/configured singleturn resolution + multiturn resolution).

Additional bits like parity, error etc. can be added on request, but this would be a customized configuration, not standard.

The position value can be transmitted in binary or gray code, depending on the ordered configuration.

Data transmission is initiated by the first falling edge of the CLK, which triggers the internal sampling. The MSB is on the Data line at the first rising edge. With each rising edge the next bit is available at the data line. One doesn't need to clock out the complete value. If you keep the CLK on high level for $t_m > 30\mu s$, the timeout t_{tp} (min $15\mu s$ / max $30\mu s$) occurs and a new position value is available. The encoder signals this by switching the Data from low to high. If CLK pauses for less than t_{tp} ($< 15\mu s$) the transmission can be continued without a problem.(see Figure 2.1)

Single transmission

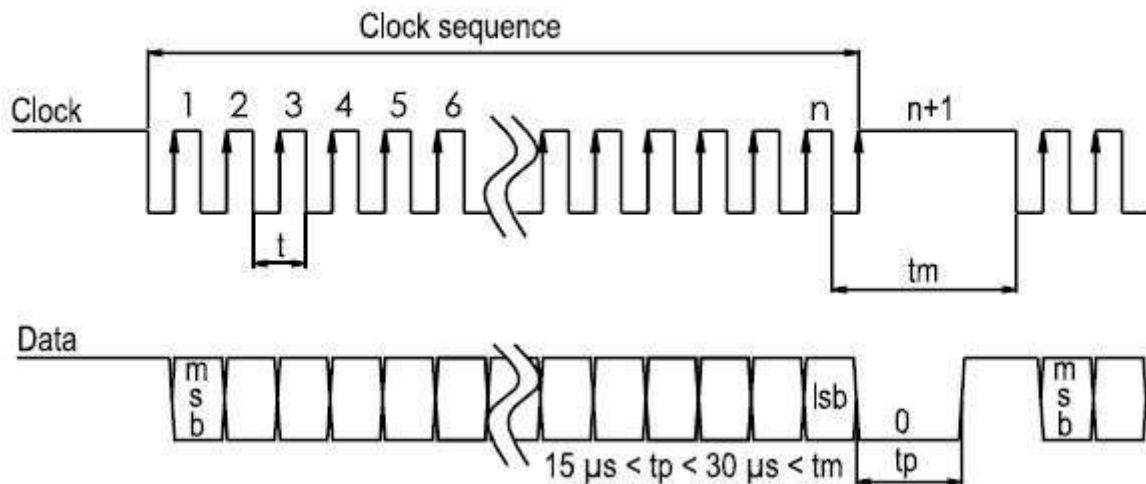


Figure 2.1: Single transmission

If one clocks out more than the length of the process data without the timeout, the old value will be send again (multiple transmission for higher security). At multiple transmissions the LSB and MSB will be separated by two low bits. (See Figure 2.2)

Multiple transmission:

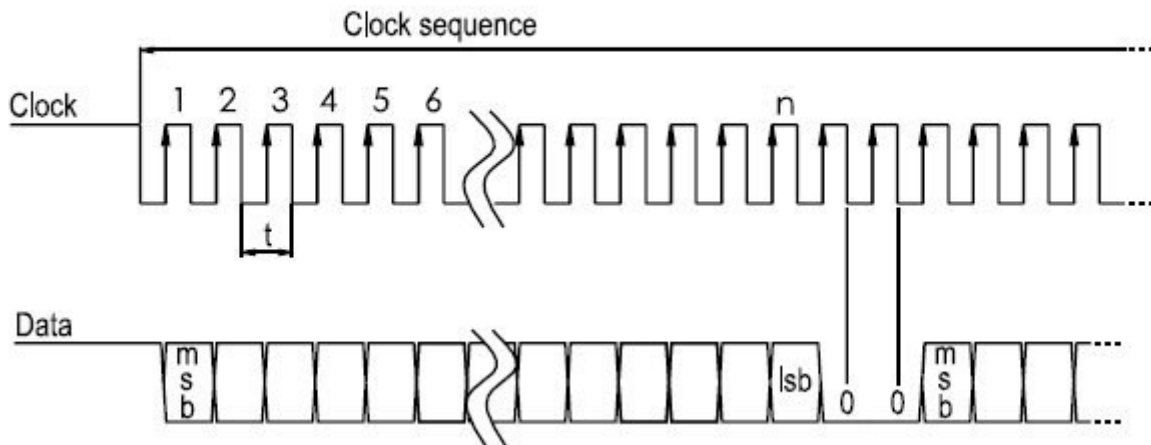


Figure 2.2: Multiple transmission

2.1. Special Option ADL

The standard WDGA encoder with SSI interface has at limited clock frequency of max 500 kHz. With respect to the internal cycle time of approx. 600µs is this not a significant limitation. A 25bit position value for example needs 52µs transmission time at 500 kHz.

For applications with a SSI master clock higher than 500 kHz Wachendorff provides the special type „ADL“ which can operate with clock rates up to 2 MHz.

The disadvantage of this variant on the other hand is a worse timeliness of the position data which can be one period older than in the standard SSI variant.

Therefore the timeout pause between two transmission frames has a direct influence how old the position value is.

The maximum cable length depends on the clock frequency, cable type and used SSI-Master. We recommend shielded twisted-pair cable. The following values can be used as guide values (see table 2.1)*:

Maximum cable length / m	Clock frequency / kHz
4	<2000
10	<1400
25	<900
50	<500
100	<250
200	=100

Table 2.1: Typical Maximum cable length

*For products with 4.5...5.5 VDC power supply maximum 2m cable length.

2.2. Special Option AEF

At multiple transmissions the LSB and MSB will be separated by one low bit. (See Figure 2.3)

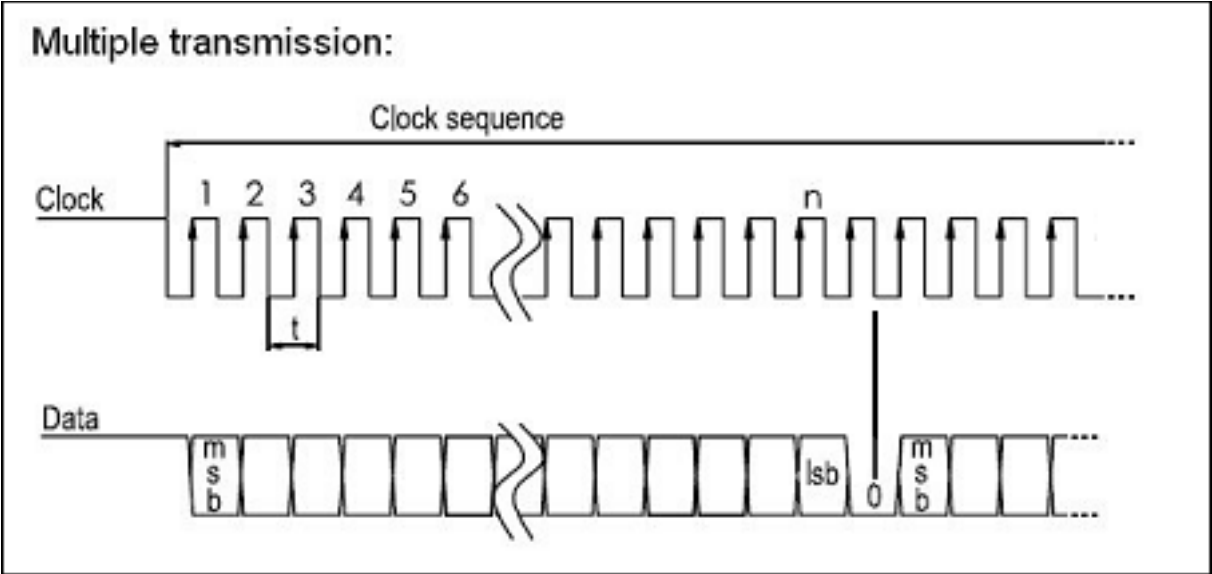


Figure 2.3: Multiple transmission with one low bit

3. Copyright

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5. Customer service and technical support

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